Re Point V

1. Reference is made to the following documents:

D1: EP 1 161 124 A (ALPS ELECTRIC CO., LTD) 5 December 2001

D2: US 6 359 331 B1 (RINEHART LAWRENCE EDWARD ET AL) 19 March 2002

D3: WO 03/030247 A (SIEMENS AKTIENGESELLSCHAFT; HAESE, KERSTIN; AMIGUES, LAURENCE; SCHWARZ) 10 April 2003

2. INDEPENDENT CLAIM 1

2.1 Notwithstanding the lack of clarity (see point VIII below, sections 1-3) the subject matter of **Claim 1** is not novel within the meaning of **Article 33(2) PCT**.
Document D1 discloses (the references in brackets relate to this document):

- A circuit arrangement placed on a substrate and comprising at least one semiconductor component arranged on the substrate and having at least one electrical contact surface (column 5, lines 33-54; column 9, lines 47-52; Figures 2 and 4) and
- at least one connection line arranged on the substrate and used to electrically contact the contact surface of the semiconductor component, said electrical connection line forming part of a discrete passive electrical component arranged on the substrate (column 7, lines 17-25; column 8, lines 4-11; column 10, lines 37-43; Figures 2, 4 and 8: the electrodes of the capacitor C6 are embodied as metal layers arranged on the substrate. It is apparent from Figure 2 that one of the metal layers serving as electrodes of the capacitor C6 also has a connection region SL which is connected to a contact terminal surface of the transistor Tr1 via a wire bond connection. This metal layer can hence be regarded as an electrical connection line which is both used to electrically contact the contact surface of the semiconductor component and also forms part of a passive component arranged on the substrate).

Document D1 thus discloses all technical features of the independent Claim 1. The subject matter of this claim is hence not novel (**Article 33(2) PCT**).

2.2 The subject matter of **Claim 1** does not, in particular in combination with the technical features set out in point VIII below, sections 1 and 2, relate to an inventive step within the meaning of **Article 33(3) PCT**.

2.2.1 Document D2 is regarded as the closest prior art compared to the subject matter of this claim. It discloses (the references in brackets relate to this document):

- A circuit arrangement placed on a substrate and comprising at least one semiconductor component arranged on the substrate and having at least one electrical contact surface (column 3, lines 15-37; Figure 4) and
- A layer arrangement with an electrical connection structure ("interconnect layer assembly" (32)) which has a connection line to electrically contact the contact surface of the semiconductor component, the connection line forming part at least of a discrete passive, electrical component which is likewise part of the layer arrangement (column 3, lines 29-43; column 4, lines 6-20 and lines 35-43; Figures 4 and 5c: Figure 5c discloses sense resistors (50) embodied in the copper layer (48) as part of a connection line with a connection hole (54) embodied in the same copper layer (48). The connection line is used to contact the contact surface of a semiconductor component via the terminal post (40)).

2.2.2 The subject matter of Claim 1 hence differs from the one known from D2 in that

- the layer arrangement is embodied on the substrate with at least one semiconductor component arranged on the substrate and the layer arrangement consists at least of the electrical connection line mentioned in section 2.2.1 above and arranged on the substrate. As regards the

expression "*arranged on the substrate*", reference is also made to the objection as to clarity cited in the following point VIII, section 3.

2.2.3 The object to be achieved with the present invention can thus be deemed to be to achieve a more compact structure of the circuit arrangement with increased reliability of the electrical connections.

2.2.4 **Document D3** likewise discloses in Claims 1, 2, 11, 12 and Figure 2 a circuit arrangement on a substrate, comprising semiconductor components arranged on the substrate and electrically insulating plastic films laminated onto this arrangement. There is a metal layer between these films in each case. These metal layers are used for contacting the semiconductor components and for interconnecting the semiconductor components (see D3: page 7, line 34 – page 8, line 4). The contact surfaces of the semiconductor components are here contacted flat directly by the metal layers (see D3: page 12, lines 1-15; Figure 2).

2.2.5 The person skilled in the art would hence use the connection technology disclosed in D3 to electrically contact and connect terminal contact surfaces for the substrate known from D2 with the at least one semiconductor component and replace the layer arrangement (32) in D2, while retaining the electrical functionality, by the layer arrangement known from D3 and arranged directly on the substrate without inventive activity in order to achieve the stated object (in this connection, see also the advantages of this connection technology cited in D3: page 8, lines 30-36). He would then achieve a circuit arrangement according to the independent Claim 1 without having to take an inventive step (**Article 33(3) PCT**).

2.2.6 In addition he would select the number, sequence and structure of the electrically insulating plastic films and of the metal layers to suit the circumstances, in order to obtain the desired electrical connection structure. This is a common design measure for the person skilled in the art, which cannot be regarded as inventive (**Article 33(3) PCT**).

2.2.7 The subject matter of the independent Claim 1 hence does not relate to an inventive step within the meaning of **Article 33(3) PCT**.

3. DEPENDENT CLAIMS 2-7

Claims 2-7 do not contain any features which in combination with the features of any claim to which they relate fulfill the requirements of the PCT with respect to novelty or inventive step.

3.1 **Claim 2**: See **D1**: Figure 2 and section 2.1 above (**Article 33(2) PCT**).

3.2 **Claim 4**: See **D2**: column 4, lines 18-20; Figure 4 and sections 2.2.1 – 2.2.5 above (**Article 33(3 PCT**).

3.3 **Claims 3 and 5**:

The technical features for the integral embodiment of the discrete passive electrical components cited in these claims, whereby a connection line arranged on the substrate forms part of the passive component, are known to the person skilled in the art. Thus for example the component could form an integral part of a layer arrangement of electrically conductive and electrically non-conductive layers, whereby the component is implemented for example on or in a substrate coated with electrically conductive layers. The substrate can here itself comprise a layer arrangement (**Article 33(3) PCT**).

The person skilled in the art would hence select such an integral construction for the passive component to suit the circumstances, in order to achieve the object proposed (**Article 33(3) PCT**).

The technical features of Claims 3-5 (and additionally for the same reason the features of Claims 2 and 4) cannot therefore, in combination with the features of the independent Claim 1, substantiate an inventive

step (**Article 33(3) PCT**).

3.4 **Claims 6 and 7**:

See **D2**: column 3, lines 26-31; Figure 2 (**Article 33(3) PCT**).
The features of this claim are additionally unable, in combination with the features of the independent Claim 1, to substantiate an inventive step compared to the circuit arrangements disclosed in Documents **D1 – D3** (**Article 33(3) PCT**).

4. INDEPENDENT CLAIM 8 AND DEPENDENT CLAIMS 9, 10

4.1 **Document D2** is regarded as the closest prior art compared to the subject matter of these claims and discloses the method feature that when creating the electrical connection line the part of the discrete passive electrical component is produced (the connection line and the sense resistor (50) are embodied in a common copper layer (48), see in this respect also section 2.2.1 above and D2: Figure 5c; it is generally usual for the person skilled in the art to embody these elements in a single method step by structuring the copper layer (48); this feature is hence implicitly disclosed).

4.2 **Claims 8 and 10:**

In **sections 2.2.2 – 2.2.5 above** it was explained that the person skilled in the art would use the connection technology disclosed in **Document D3** for the circuit arrangement known from D2 without inventive activity in order to achieve the stated object. It is an obvious action for the person skilled in the art and it represents a normal procedure for him also to take over for this purpose the method steps of the disclosed connection technology specified in D3 for producing the connection structure (see D3: Claims 1, 2, 11 and 12; Figures 1 and 2). Thus he would arrive at

the subject matter of Claims 8 and 10 without thereby taking an inventive step (**Article 33(3)PCT**).

4.3 **Claim 9**:

For the person skilled in the art it is an obvious method variant, generally known to him, to apply the layer of electrically insulating material so that the electrical contact of the semiconductor component located underneath the layer is freely accessible. Hence this feature cannot, in combination with the features of the independent Claim 8, to which Claim 9 refers back, substantiate an inventive step (**Article 33(3) PCT**).

4.4 The subject matter of **Claims 8-10** hence does not relate to an inventive step within the meaning of **Article 33(3) PCT**.

4.5 Nor does the subject matter of these claims relate to an inventive step within the meaning of **Article 33(3) PCT** compared to a combination of the features of these claims with the features explained in point VIII below, sections 1 and 2, since these features are known from **D3** (see D3: Claims 1, 2, 11 and 12; Figures 1 and 2).

5. Claims 1-10 fulfill the requirements of Article 33(4) PCT, since they are susceptible of industrial application.

Re Point VIII

1. It emerges from the description on page 3, paragraph 1 and page 4, paragraph 3, that the following features are essential for the definition of the invention:
   (a) The electrical contact surface of the semiconductor component faces away from the substrate.
   (b) The electrical connection line contacts the electrical contact surface of the semiconductor element.

   Since the **independent Claim 1** does not contain the **feature (a)** and the

independent Claims 1 and 8 do not contain the **feature (b)**, the independent claims do not fulfill the requirement of **Article 6 PCT in conjunction with Rule 6.3 b) PCT** that every independent claim must contain all technical features which are essential for the definition of the invention.

2. Only circuit arrangements and production methods for circuit arrangements that have the following features can be derived from the present international application:

- An electrically insulating layer is applied to the substrate with the semiconductor component.
- The connection line is a metal layer arranged on this electrically insulating layer.

Since the **independent Claims 1 and 8** do not have corresponding technical features, **the present application is not, as laid down in Article 6 PCT, fully supported by the description and the drawings of the present international application**, since the scope of these claims goes beyond the scope justified by the description and the drawings.

3. Because of the wording of this claim and the circuit arrangements disclosed in the description and the drawings of the international application and the production methods for circuit arrangements, the meaning of the expression "*arranged on the substrate*" used in the **independent Claim 1** is not clear:

Thus for example it is apparent from the present application, Figure 1, and from the description on page 10, line 33 – page 11, line 17 that the semiconductor component (3) is arranged on a copper layer (22) of a DBC substrate (2), whereas the connection line (4) is applied to an electrically insulating film (6) and thus not directly to the DBC substrate (2). According to the wording of Claim 1, however, both the semiconductor component and the connection line are arranged on the substrate. This circumstance gives rise to doubts regarding the application for

protection, in particular which components are arranged directly on the substrate (**Article 6 PCT**).

Furthermore the expression "*arranged on the substrate*" could also be understood to mean that the connection line, in contrast to the exemplary embodiment mentioned previously, is arranged on the copper layer (22) of the DBC substrate, as with the semiconductor component (3), without a further insulating layer located between component and copper layer (**Article 6 PCT**).

4. The **independent claim 8** is not clear, since the wording used in this claim "... *and the part of the discrete passive electrical component being produced*" gives the impression that this component was defined in greater detail previously. This gives rise to doubts regarding the application for protection, so that the subject matter of this claim is not clear (**Article 6 PCT**).